Q.P.Code: **20EC0442** | R20 | **H.T.No.**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech. IV Year I Semester Regular & Supplementary Examinations October/November-2025
VLSI DESIGN
(Electronics & Communications Engineering)

Time: 3 Hours **Max. Marks: 60**

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	a	Summarize the evolution of microelectronics.	CO1	L2	6M
	b	Explain working of the NMOS transistor.	CO1	L2	6M
		OR			
2	a	What are the different forms of Pull Up Loads? Which is the best choice for realization?	CO2	L1	6M
	b	Derive the expression for threshold voltage for MOS transistors.	CO2	L3	6M

UNIT-II

3	a	Explain the steps involved in VLSI Design flow.	CO3	L2	6M
	b	Construct the stick diagram of a 2-input CMOS NAND gate.	CO3	L3	6M
		OR			
4	a	Illustrate stick diagram of AND-OR-INVERTER in CMOS design Style	CO3	L2	6M
	b	Explain about Implant and demarcation line in stick diagrams with neat Sketches.	CO3	L2	6M

UNIT-III

5	a	Draw the CMOS implementation of 4X1 mux using transmission gates?	CO4	L1	6M
	b	Explain pseudo NMOS logic gate?	CO4	L2	6M
		OR			
6	a	What design methods are used in physical design cycle? Explain each term with suitable diagrams.	CO4	L1	6M
	b	What is routing? Explain about different routing techniques.	CO4	L2	6M

UNIT-IV

7	a	Define the Counters in the digital circuit. Design 4-bit Asynchronous counter.	CO6	L1	6M
	b	Define Parity generator logic circuits. Design 4-bit Parity generator using EX-OR gate.	CO6	L3	6M
		OR			
8	a	Construct and explain the circuit diagram of 3-bit LFSR with example.	CO6	L3	6M
	b	Construct and explain the Johnson counter.	CO6	L3	6M

UNIT-V

9	a	Compare PROM, PAL, and PLA with an example.	CO5	L1	6M
	b	Design the PAL Structure for the Boolean function f1(a,b,c,d)=ab+bc & f2(a,b,c,d)=ab+cd	CO5	L3	6M
		OR			
10	a	What is testing? Explain any three test principles.	CO5	L1	6M
	b	What is controllability and observability? Give examples to explain it.	CO5	L2	6M

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